EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 3

2/14/24 - 2/20/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

This week, we were able to run the analog design flow all the way up to LVS/parasitic extraction on a simple inverter. Discussed transimpedance amplifiers and ADCs architectures. We also went over how the computation cross bar computes matrix-vector multiplication

Past Week Accomplishments:

- Created and pushed an inverter through the analog design flow
- Installed and ran all required open-source software on Ubuntu
- Looked into ADC (Analog to Digital Converter) design methods to talk to our client and advisor about which method or what specific performance goals they would like out of the device

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Created and pushed an inverter through analog tool flow after troubleshooting and fixing tools. Researched more about how ReRAM compute works.	8	22
Gage Moorman	Created an inverter and made it all the way to DRC, researched TIA architectures and ADCs (Analog to Digital Converter).	8	22
Nathan Cook	Got inverter through DRC testing, LVS testing was not working on the toolchain at the time but does as of 2/20/24	7	21
Jason Xie	Created an inverter with provided toolchain and got to layout LVS. Gained a better understanding of ReRam Crossbar MAC. Researched different ADCs.	8	20

Pending Issues:

- Getting Inverter through parasitic simulations and finishing the analog tool flow process.
- Begin work on digital tool flow using inverter as a hello world example
- Decide on type of ADC and DAC we will use for the process
    - Still must figure out how we can maximize resolution while also minimizing the space taken
    - DAC design will be affected by what type we choose as well
- Begin work on getting instruction set for the crossbar in order and on its way to being built
    - Need to check with client and advisor if the instruction set is needed as of now

Plans for the coming week:

- Gage Moorman
    - Discuss and decide on ADC architecture as well as TIA structures
    - Finish inverter LVS and parasitic extraction
    - More research into ReRAM and memristors
- Konnor Kivimagi
    - Reasearch different ADC and DAC architectures to begin thinking about and designing the one that works best for us.
    - Reasearch ReRAM and try to patch any holes in my knowledge
    - Spend some time really ironing out any kinks in the tool flow
        - Possibly documenting any changes from current documentation for future use
- Nathan Cook
    - Finish getting inverter through tool flow, from LVS onwards
    - Start on instruction set
    - Keep researching ReRAM, ADC, and DAC technology
        - Multiple papers and articles are pinned for reading
- Jason Xie
    - Finish practicing with analog design flow process
    - Begin looking into digital design flow regarding crossbar representation
    - Assist in researching ADC and DAC architectures

Summary of Advisor Meeting:

During our meeting this week, we went over how the ReRAM writes to memory, the functions that need to be included and more specifics on how the cells are weighted, specifically their use of the 1T1R scheme for the memory cells. Following this we spoke more about what this would entail for the ADC and DAC functions as well as the challenges that would come with it, being able to read and write at the same time as well as figuring out what values are in what cells by using the current.